Nothing Found

Your search for **"Daren Dance"** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

```
sales offices
```

  You can also enter a full question or concept in plain language.

```
Where are the sales offices?
```

- Capitalize proper nouns to search for specific people, places, or products.

```
John Colter, Netscape Navigator
```

- Enclose a phrase in double quotes to search for that exact phrase.

```
"museum of natural history" "museum of modern art"
```

- Narrow your searches by using a + if a search term must appear on a page.

```
museum +art
```

- Exclude pages by using a - if a search term must not appear on a page.

```
museum -Paris
```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Nothing Found

Your search for **"David Jimenez"** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

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  sales offices
  ```

  You can also enter a full question or concept in plain language.

  ```
  Where are the sales offices?
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  John Colter, Netscape Navigator
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  "museum of natural history" "museum of modern art"
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  ```
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  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Nothing Found

Your search for **"IDC Systems Inc"** did not return any results.

You may want to try an Advanced Search for additional options.

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Quick Tips

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John Colter, Netscape Navigator
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museum -Paris
```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Terms used **production efficiency wafers tool groups time percentage**

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Relevance scale

1 Semiconductor manufacturing: factory simulation: Economy of scale effects for large wafer fabs

Oliver Rose

December 2006 **Proceedings of the 37th conference on Winter simulation WSC '06**

Publisher: Winter Simulation Conference

Full text available: pdf(177.07 KB) Additional Information: full citation, abstract, references

In this paper, we present the results of a simulation study for semiconductor wafer fabrication facilities (wafer fabs) where we multiplied the number of tools per tool group and the number of operators. We were interested in the effects on the product cycle times when we keep the fab utilization constant while increasing the size of the tool groups by constant factors, i.e., forming so-called giga fabs. It turns out, that the drop in cycle time is considerable.

2 An investigation of operating methods for 0.25 micron semiconductor manufacturing

James F. Hallas, Jane D. Kim, Charles T. Mosier, Carolyn Internicola

November 1996 **Proceedings of the 28th conference on Winter simulation WSC '96**

Publisher: ACM Press, IEEE Computer Society

Full text available: pdf(732.33 KB) Additional Information: full citation, abstract, references

This study investigates a number of operational issues associated with the control of microprocessor fabrication facilities, specifically expanding the domain of previous research to investigate the effects of lot size, test wafer proportion, and tool productivity on wafer fabrication performance. Response variables included cost and production performance metrics.

3 Semiconductor manufacturing: Semiconductor manufacturing scheduling: maximizing delivery performance in semiconductor wafer fabrication facilities

Scott J. Mason, John W. Fowler

December 2000 **Proceedings of the 32nd conference on Winter simulation WSC '00**

Publisher: Society for Computer Simulation International

Full text available: pdf(196.99 KB) Additional Information: full citation, abstract, references

This paper is motivated by the problem of scheduling customer orders (jobs) in a semiconductor fabrication facility ("wafer fab") to maximize delivery performance when the jobs have non-identical priorities (weights). As each job is typically assigned a weight based on its size, value, and/or requesting customer, a wafer fab's delivery performance

can be evaluated in terms of minimizing the sum of each job's weighted tardiness. A heuristic has been proposed for obtaining "good" solutions to this ...

4 Semiconductor manufacturing: General simulation applications in semiconductor manufacturing: why do simple wafer fab models fail in certain scenarios?
Oliver Rose
December 2000 **Proceedings of the 32nd conference on Winter simulation WSC '00**
Publisher: Society for Computer Simulation International
Full text available: pdf(116.27 KB) Additional Information: full citation, abstract, references

Previous work has proved that simple simulation models are sufficient for analyzing the behavior of complex wafer fabs in certain scenarios. In this paper, we give an example where the simple model fails to accurately predict cycle times and WIP levels of the complex model. To determine the reason for this behavior, we analyze the correlation properties of a MIMAC full fab model and the corresponding simple one. It turns out that the simple model is not capable of capturing the correlations in a ...

5 Semiconductor manufacturing: Wafer fabrication: 300mm wafer fabrication line simulation model
Sameer T. Shikalgar, David Fronckowiak, Edward A. MacNair
December 2002 **Proceedings of the 34th conference on Winter simulation: exploring new frontiers WSC '02**
Publisher: Winter Simulation Conference
Full text available: pdf(147.92 KB) Additional Information: full citation, abstract, references, citings

The importance of semiconductor wafer fabrication has been increasing steadily over the past decade. Wafer fabrication is the most technologically complex and capital intensive phase in semiconductor manufacturing. It involves the processing of wafers of silicon in order to build up layers and patterns of metal and wafer material. Many operations have to be performed in a clean room environment to prevent particulate contamination of wafers. Also, since the machines on which the wafers are pr ...

6 A model of a 300mm wafer fabrication line
Philip L. Campbell, Darius Rohan, Edward A. MacNair
December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation--a bridge to the future - Volume 1 WSC '99**
Publisher: ACM Press
Full text available: pdf(34.82 KB) Additional Information: full citation, references, citings, index terms

7 Semiconductor manufacturing: Factory scheduling and dispatching: simulation-based assessment of batching heuristics in semiconductor manufacturing
Lars Mönch, Ilka Habenicht
December 2003 **Proceedings of the 35th conference on Winter simulation: driving innovation WSC '03**
Publisher: Winter Simulation Conference
Full text available: pdf(383.58 KB) Additional Information: full citation, abstract, references

In this paper, we investigate the performance of different dispatching and scheduling heuristics for batching tools in a semiconductor wafer fabrication facility (wafer fab) by means of discrete event simulation. Because the processing times of lots on batching tools are quite large compared to those of other processes, careful batching decisions may have a great impact on the performance of the entire wafer fab. In a first step, we investigate the performance of certain modifications of the ...

8 Integrating targeted cycle-time reduction into the capital planning process
Navdeep S. Grewal, Alvin C. Bruska, Timbur M. Wulf, Jennifer K. Robinson
December 1998 **Proceedings of the 30th conference on Winter simulation WSC '98**
Publisher: IEEE Computer Society Press
Full text available: pdf(60.23 KB) Additional Information: full citation, references, citings, index terms

9 Semiconductor manufacturing: Scheduling and dispatching: a finite-capacity beam-search-algorithm for production scheduling in semiconductor manufacturing
Ilka Habenicht, Lars Mönch
December 2002 **Proceedings of the 34th conference on Winter simulation: exploring new frontiers WSC '02**
Publisher: Winter Simulation Conference
Full text available: pdf(207.71 KB) Additional Information: full citation, abstract, references, citings

In this paper we describe a finite-capacity algorithm that can be used for production scheduling in a semiconductor wafer fabrication facility (wafer fab). The algorithm is a beam-search-type algorithm. We describe the basic features of the algorithm. The implementation of the algorithm is based on the ILOG-Solver libraries. We describe the simulation environment, which is used to evaluate the performance of the proposed algorithm. We show some results from computational experiments with the ...

10 Semiconductor manufacturing: A simulation-based cost modeling methodology for evaluation of interbay material handling in a semiconductor wafer fab
Shari Murray, Gerald T. Mackulak, John W. Fowler, Theron Colvin
December 2000 **Proceedings of the 32nd conference on Winter simulation WSC '00**
Publisher: Society for Computer Simulation International
Full text available: pdf(2.08 MB) Additional Information: full citation, abstract, references, citings

In the next generation of semiconductor wafer fabrication facilities, decisions concerning material handling systems will be a major factor in initial facility cost, operational cost, production cycle times, and possibly product yield percentages. The wafers will increase in diameter to 300 mm and a new front opening unified pod (FOUP) has been designed to carry them, both increasing the weight of a production lot. This increase requires substantial automation for ergonomic and quality reasons. ...

11 Operational simulation of an x-ray lithography cell: comparison of 200mm and 300mm wafers
K. Preston White, Walter J. Trybula
December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation--a bridge to the future - Volume 1 WSC '99**
Publisher: ACM Press
Full text available: pdf(138.94 KB) Additional Information: full citation, references, index terms

12 Semiconductor manufacturing: Simulation-based solution of load-balancing problems in the photolithography area of a semiconductor wafer fabrication facility
Lars Mönch, Matthias Prause, Volker Schmalfuss
December 2001 **Proceedings of the 33nd conference on Winter simulation WSC '01**
Publisher: IEEE Computer Society
Full text available: pdf(230.41 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present the results of a simulation study for the solution of load-balancing problems in a semiconductor wafer fabrication facility. In the bottleneck area of

photolithography the steppers form several different subgroups. These subgroups differ, for example, in the size of the masks that have to be used for processing lots on the steppers of a single group. During lot release it is necessary to distribute the lots over the different stepper groups in such a way that global targ ...

13 Semiconductor manufacturing: Wafer fabrication: effects of metrology load port buffering in automated 300mm factories

Robert Wright, Marlin Shopbell, Kristin Rust, Silpa Sigireddy

December 2002 **Proceedings of the 34th conference on Winter simulation: exploring new frontiers WSC '02**

Publisher: Winter Simulation Conference

Full text available: pdf(184.80 KB) Additional Information: full citation, abstract, references

This report describes a simulation study characterizing the advantages and disadvantages of implementing multiple load ports on metrology equipment in a semiconductor factory. Three methods of automated material handling (AMH) for 300 mm wafer carriers in four separate models were analyzed: Through Stocker, Point-to-Point, and Conveyor (slow and fast velocity). Parameters measured include idle times of metrology equipment as number of load ports change and the effects on bottleneck equipment, ...

14 Semiconductor manufacturing: semiconductor factory scheduling and control: Comparative factory analysis of standard FOUP capacities

Kranthi Mitra Adusumilli, Robert L. Wright

December 2004 **Proceedings of the 36th conference on Winter simulation WSC '04**

Publisher: Winter Simulation Conference

Full text available: pdf(262.08 KB) Additional Information: full citation, abstract, references

Wafers in a 300-mm semiconductor fabrication facility are transported throughout the factory in carriers called front opening unified pods (FOUPs). Two standard capacities of FOUPs are 25 and 13 wafers. This paper describes a simulation study designed to compare the performance of a factory employing different FOUP capacities. The main performance measure considered is work-in-process (WIP) and the resulting cycle time. Batching policy, order arrival rate, average order size, the Automated Mater ...

15 Semiconductor manufacturing: performance analysis in semiconductor manfacturing: Simulation analysis on the impact of furnace batch size increase in a deposition loop

Boon Ping Gan, Peter Lendermann, Kelvin Paht Te Quek, Bart van der Heijden, Chen Chong Chin, Choon Yap Koh

December 2006 **Proceedings of the 37th conference on Winter simulation WSC '06**

Publisher: Winter Simulation Conference

Full text available: pdf(267.36 KB) Additional Information: full citation, abstract, references

In the dynamic environment of semiconductor manufacturing operations, a bottleneck could be created at the bake furnaces of the deposition loop as capacity expands. Upgrading of the bake furnaces by adding a lot-per-batch in the boat or purchasing a new furnace are two possible solutions to this problem. A simulation model was constructed to assist the decision making, with the behavior of the wet benches (upstream tools) and cluster tools (downstream tools) being modeled in detail. We concluded ...

16 Semiconductor manufacturing: factory simulation: Efficient simulations for capacity analysis and automated material handling system design in semiconductor wafer fabs

Jesus A. Jimenez, Gerald Mackulak, John Fowler

December 2005 **Proceedings of the 37th conference on Winter simulation WSC '05**

Publisher: Winter Simulation Conference

Full text available: pdf(199.91 KB) Additional Information: full citation, abstract, references

The Automated Material Handling System (AMHS) must be designed effectively so that it never becomes a limiting factor for the capacity of 300mm wafer fabs. Ideally, a fully integrated fab simulation model (i.e. a model containing detailed modeling constructs for the production operations, the tools, the AMHS, and tool AMHS interactions) should be used in order to design the AMHS. However, the problem is that it takes too much time to simulate and analyze these models. Experimentation has demonst ...

17 A comparison study of the logic of four wafer fabrication simulators

Scott J. Mason, Paul A. Jensen, John W. Fowler

November 1996 **Proceedings of the 28th conference on Winter simulation WSC '96**

Publisher: ACM Press, IEEE Computer Society

Full text available: pdf(796.00 KB) Additional Information: full citation, abstract, references, citings

Many semiconductor manufacturing companies use one of the following four simulators to aid in analyzing, planning, and operating their manufacturing facilities: Tyecin Systems' ManSim/X, AutoSimulations' AutoSched, Systems Modeling's Wafer Fabrication Template, or Chance Industrial Solution's Delphi, which Wright, Williams, and Kelly now licenses as Factory Explorer. A benchmark study of the four packages was conducted, using actual factory data. The packages each produce different results betwe ...

18 Semiconductor manufacturing: dispatching and scheduling approaches: Simulation-based selection of machine criticality measures for a shifting bottleneck heuristic

Jens Zimmermann, Lars Mönch

December 2006 **Proceedings of the 37th conference on Winter simulation WSC '06**

Publisher: Winter Simulation Conference

Full text available: pdf(243.98 KB) Additional Information: full citation, abstract, references

In this paper, we investigate the influence of several machine criticality measures on the performance of a shifting bottleneck heuristic for complex job shops. The shifting bottleneck heuristic is a decomposition approach that tackles the overall scheduling problem by solving a sequence of tool group scheduling problems and composes the overall solution by using a disjunctive graph. Machine criticality measures are responsible for the sequence of the considered tool group scheduling problems. W ...

19 Capacity planning for semiconductor wafer fabrication with time constraints between operations

Jennifer K. Robinson, Richard Giglio

December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation---a bridge to the future - Volume 1 WSC '99**

Publisher: ACM Press

Full text available: pdf(93.05 KB) Additional Information: full citation, references, citings, index terms

20 Simulation-based scheduling: Semiconductor manufacturing: ASAP applications of simulation modeling in a wafer fab

Kishore Potti, Amit Gupta

December 2002 **Proceedings of the 34th conference on Winter simulation: exploring new frontiers WSC '02**

Publisher: Winter Simulation Conference

Full text available: pdf(142.98 KB) Additional Information: full citation, abstract, references

The authors define 4 levels of complexity in simulation modeling. The ability of the models to predict bottlenecks in the fab. Capability of the model to be used for strategic applications such as cycle time reduction. Simulate complex dispatch rules using the

model, Capability of the model to predict operational output of the wafer fab that is clean room outs by product by day. This paper presents the operational applications of the ASAP simulation model to provide wip flush to the test prob ...

Results 1 - 20 of 49 Result page: **1** 2 3 next

	Type	L #	Hits	DBs	Search Text	Time Stamp
1	BRS	L1	1	USPAT	"6170081".pn.	2007/05/08 09:03
2	BRS	L2	1	USPAT	"6170081".pn. and time	2007/05/08 09:04
3	BRS	L6	236	USPAT	(calcula$6 same production same tools)	2007/05/08 09:44
4	BRS	L7	16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(calcula$6 same production same tools same groups)	2007/05/08 09:44
5	BRS	L8	116	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(calcula$6 same production same tools same groups)	2007/05/08 09:44
6	BRS	L9	15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	(calcula$6 same production same tools same groups) and "700"/$.ccls.	2007/05/08 09:47
7	BRS	L10	74	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	700/121.ccls. and (production same calculation)	2007/05/08 09:48

Interference

	Type	L #	Hits	DBs	Search Text	Time Stamp
1	BRS	L1	0	US-PGPUB	(production same quanitity same tools)	2007/05/08 16:00
2	BRS	L2	1	US-PGPUB	(production same quanitity) and tools	2007/05/08 16:00
3	BRS	L3	520	US-PGPUB	(tools same groups same time)	2007/05/08 16:01
4	BRS	L4	9	US-PGPUB	(tools same groups same time same wafer)	2007/05/08 16:01
5	BRS	L5	120	US-PGPUB	(wafer$3 or semiconductor) same groups same tools	2007/05/08 16:01

TS